Analysis of Error Sources in Electrical Circuits and Accuracy Improvement of Electrical Devices

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Abstract: The accurate and reliable operation of electrical equipment is a fundamental requirement for their application in precision engineering. Simple error formulas allow the easy establishment of functional interdependencies between outputs and input quantities. Analytical methods enable sensitivity analysis to be performed successfully and with relative ease when these dependencies are explicitly given, or when combined with experimental techniques for application in more complex scenarios. However, accurately testing inherently non-linear devices poses serious challenges, particularly when it comes to going beyond simple accuracy characterization and into active error source correction. These issues are the primary obstacles in defining a general engineering framework that uses possible modeling, calculation, and optimization approaches for irregular complex non-linear systems. The present paper presents a systematic approach to error sources in secondary power supply units, especially within functional converters with a building block made up of passive non-linear elements and supplied from DC. The method builds on constructing a causal graph of a magneto-transistor voltage divider and analyzing circuit segments in relation to their voltage dividing properties. This graphical representation comes with significant simplicity, clarity, and interpretability benefits that should enable easier recognition of primary error contributors. The presented approach is not only capable of identifying sensitivity coefficients accurately, even under certain non-linear operating conditions, but also allows for directed error compensation. These results are anticipated to provide a basis for the development of engineering methodologies in precision electrical device and system design and optimization.

1 INTRODUCTION

The process of improving the accuracy of electrical circuits is the acquisition, collection, transmission and processing of information on their operating and structural states, aimed at eliminating deviations of real processes from ideal ones.

The first step in device design, research and error correction is to formulate requirements for device accuracy and other metrics.

The second stage is the selection of the structure and mode of the device. At this stage, many principles of device structures and modes are known.

The third step consists of an analysis of the accuracy characteristics of the devices, i.e. a detailed analysis of the sources of device errors, systematized on the basis of known circuit theory methods.

The fourth step compares the compliance of the devices with the specified accuracy requirements. If the accuracy requirements are not met, then mode error correction methods are applied [1]-[3].

Mode-based methods for improving accuracy can be stand-alone or system-based. In the first case, the device to be designed is considered in isolation from the statistical characteristics of the input signal and the characteristics of the consumer. In this method, the design is reduced to the selection of mode

parameters that ensure a minimum resultant error. The essence of the system method of error analysis is that not only the parameters and characteristics of devices, but also the statistical characteristics of the input signal and the law of signal conversion at the output of the device are taken into account in a complex. At the same time the minimization of functionals is achieved, i.e. generalized accuracy criteria, which include both parameters of devices and characteristics and parameters of a signal source and load [4], [5].

Structural methods of improving device accuracy are based on changing device structures. At the same time, device accuracy improvement can be achieved by autonomous (local) or system (automatic) correction methods [9]. Local methods of introducing device accuracy correction are of interest from the point of view of simplicity, as well as acceptable technical and economic indicators. Local accuracy improvement methods considered on the basis of causal graphs (CGs), which are of interest due to their clarity and simplicity, are given in [16]. Structural-mode methods for improving accuracy are a combination of two methods: structural and mode methods. Increased accuracy of devices can be achieved by these methods. But they differ in the complexity of structural, mode optimization and hardware implementation. Structural methods of improving accuracy are based on improving the quality of manufacturing, assembly and assembly of devices [10].

2 METHODS

The error corrections of the devices can be different, depending on the factors affecting the accuracy of the device. In particular, these are automatic correction methods [2], [3]. One possible variant of such error correction for non-linear circuits with the help of their CGs is considered in this paper.

Based on the CGs, local error corrections for devices can be divided into vertex (per vertex) and route (per route);

Data on the structure of multi-linked circuits based on the laws of electrical circuits and logic algebra are used as preknown information for the construction of a device CGs.

Let's consider the basic idea of this technique using the following simple electromagnetic circuit with non-linear inductance [6], [7], [8], [12] (Fig. 1). The CGs of this circuit is shown in Figure 2.

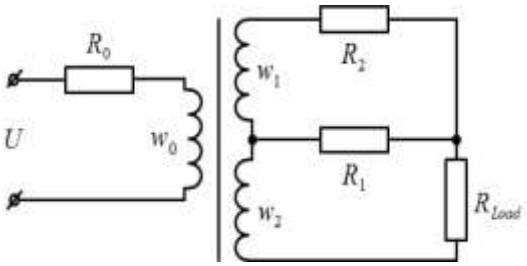

Figure 1: Section of an electromagnetic circuit with non-linear inductance.

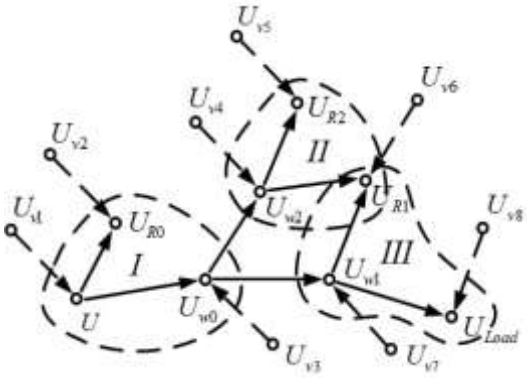

Figure 2: Causal graph of an electromagnetic circuit.

Using the above CGs, we will identify the following sources of error in the electromagnetic circuit:

1) Errors arising from direct transmission of information. They comprise the set of P_1 nodes of the graph (except for the nodes representing power sources, input and reference signals):

$$P_1 = \{U_{w_0}, U_{w_1}, U_{w_2}\}$$

2) Errors occurring in uninformative vertices of a graph. They are represented by a set of P2 vertices:

$$P_2 = \{U_{R_0}, U_{R_1}, U_{R_2}\}$$

3) Errors due to non-ideal input and reference sources and power supplies:

$$P_3 = \{U, U_{Load}\}$$

4) Errors due to external disturbances. They comprise the set of perturbing vertices P4:

$$P_4 = \{U_{v_1}, U_{v_2}, \ldots, U_{v_8}\}$$

The sets P_1 and P_2 are sources of instrumental error, P_3 is a source of transformed error, and P_4 is a source of additional electromagnetic circuit error.

This methodology for investigating the accuracy of devices using CGs allows the most significant

sources of error to be identified and ways of eliminating them to be found for each specific circuit design and operating conditions [11].

The ideal transformation of information by the vertices of the CGs ensures the accuracy of the electromagnetic circuit parameters. The following expression is then valid for the input of this circuit, based on Kirchhoff's II-law:

$$U_{\mathrm{i}} = U_{R_0\mathrm{i}} + U_{w_0\mathrm{i}} \quad (1)$$

where the index "i" denotes the ideality of the graph vertices.

In reality, in a real circuit, due to the presence of external disturbing factors (dummy vertices of the graph), there are certain errors in the chain sections and for this case (1) takes the form

$$U_{\mathrm{r}} = U_{R_0\mathrm{r}} + U_{w_0\mathrm{r}}; \quad (2)$$

where the index "r" denotes the reality of the graph vertices.

The difference of the two (1) and (2) has the following form:

$$U_{\mathrm{r}} - U_{\mathrm{i}} = \left(U_{R_0\mathrm{r}} - U_{R_0\mathrm{i}}\right) + \left(U_{w_0\mathrm{r}} - U_{w_0\mathrm{i}}\right) \quad (3)$$

Let's denote:

$$\delta = U_{\mathrm{r}} - U_{\mathrm{i}}; \;\; \delta_{R_0} = U_{R_0\mathrm{r}} - U_{R_0\mathrm{i}};$$

$$\delta_{w_0} = U_{w_0\mathrm{r}} - U_{w_0\mathrm{i}}$$

which are the absolute dynamic uncertainties of the individual vertices of the CGs.

Then (3) has the following expression for this case:

$$\delta = \delta_{R_0} + \delta_{w_0}. \quad (4)$$

Similarly, the same expressions can be obtained for the other vertices of the electromagnetic circuit graph.

Let us introduce the notion “generalized vertex” that combines the main vertex (cause) and adjacent vertices (consequence) of the graph whose arcs originate from the main vertex. Figure 2 shows generalized vertices by dashed lines.

It follows from (1), (2), (3) and (4) that for dynamic errors of generalized vertices of the graph the second Kirchhoff's law is valid.

In the case where the generalized vertices are the currents of an electromagnetic circuit, it can be proved that Kirchhoff's 1st law is valid with respect to the dynamic errors in them. In this case, the vertices of the CCGs are the branch currents of the circuit.

Therefore, for generalized graph vertices, except for vertices with "purely" logical connections, the proof "the errors of generalized CGs vertices of electrical devices with circuits obey the corresponding laws of electric circuits, i.e. Kirchhoff's laws" is valid [14].

The presence of such an error relationship in the "generalized vertices" of the graph allows for error correction of the uninformative vertices of the graph. By investigating the influence of a specific "generalized vertex" of the graph on accuracy of devices, the laws of variation of static components of errors of the generalized vertex are determined. In this case, the correction should be performed on uninformative vertices adjacent to the "generalized vertex". The influence of this correction on the main informative vertex of the graph occurs according to the specified laws of electric circuits.

Therefore, the technique of investigating the accuracy of parameters of non-linear electromagnetic circuits with the help of CGs allows, for each specific circuit solution and operating conditions, to identify the most significant sources of errors and determine the ways of their elimination [7], [9].

3 RESULTS

As stated, the errors of electrical and electronic devices, caused by the vertices of their CCGs in a "generalized vertex", obey the laws of electrical circuits.

This makes it possible to develop a methodology for automatic error correction and an accuracy test system based on the CGs of the transducers.

One of possible structural schemes of automatic error correction of functional converters (FCs) and their accuracy test system based on their CGs is shown in Figure 3 [12].

An "ideal model" of the FCs vertices is created by an exemplary computing device (CD), which implements the corresponding algorithms of the FCs chain incident matrix based on computational formulas. U_{in_n} input signals are applied simultaneously to the FCs and CD inputs. The outputs of these devices are connected to subtraction devices, the outputs of which produce vertex errors $\{\delta_{v1}, \delta_{v2},\ldots\delta_{\mathrm{vn}}\}$ CGs, can simultaneously arrive at the additional inputs of the CD and the display system. The presence of the CD incident matrix allows the total error of the FCs to be calculated; which is subtracted from U'_{out}. Given this automatic correction, the output of the FCs results in a $U_{\mathrm{out}} = F(U_{\mathrm{in1}}, U_{\mathrm{in2}},\ldots, U_{\mathrm{inn}})$ close to the "ideal model" of the FCs characteristic. The structural

diagram also allows local corrections to be realized by the device's CGs vertices. For this purpose the set of errors $\{\delta_{v1}, \delta_{v2},...\delta_{vn}\}$ are fed to the display system (DS). The obtained laws of error variation allow to identify the most significant sources of errors and find ways to eliminate them.

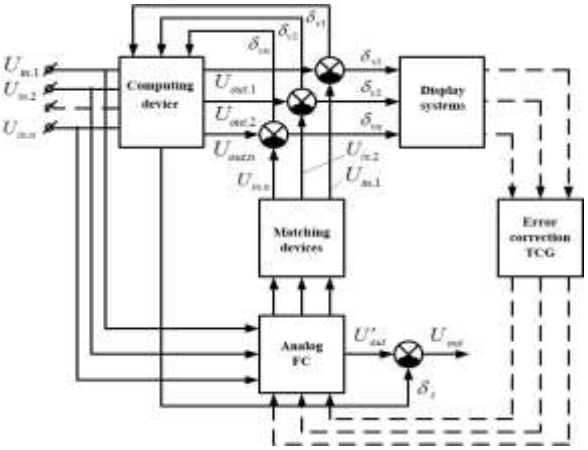

Figure 3: Structure diagram of the automatic error correction and accuracy test based on CGs FCs.

Due to this structure, conducting experimental investigations in various operational modes it is possible to determine the most vulnerable places of FCs in terms of accuracy characteristics, i.e. it is possible to estimate the parametric reliability and stability of devices or their individual elements in their interaction.

The possibility of introducing correction by individual vertices of CGs devices using the given structure gives also an opportunity to develop new FCs of increased accuracy, the basis of which are the investigated devices.

Let's consider application of CGs [11], [12] to the analysis and systematization of sources of errors of nonlinear electromagnetic circuits by the example of a single half-period magnetic-transistor dividing device (MTDD) (Fig. 4) [11], which CGs is shown in Figure 5.

For such a CG, the following system of statements is valid (without taking into account the "fictitious" vertices representing external perturbing factors), which describes the logical connection between the MTDD CG vertices [11]:

$$\left.\begin{array}{l} U_2 \Rightarrow U_{wy} \vee U_{R1} \vee U_{r2};\ U_2 \,\&\, U_\omega \Rightarrow U_{K1}; \\ U_{wy} \Rightarrow U_{wk} \,\&\, U_{wb}(\theta_s);\ U_{wk} \,\&\, U_\omega \Rightarrow U_{K2}; \\ U_{wk} \,\&\, U_\omega \Rightarrow U_{K2};\ U_2 \,\&\, U_{wK} \Rightarrow U_{r2}; \\ U_{wb}(\theta_S) \Rightarrow U_{Sm}(\theta_S) \vee U_{rb}; \\ U_1 \,\&\, U_{Sm}(\theta_S) \Rightarrow U_N \vee U_{EKN}. \end{array}\right\} \quad (5)$$

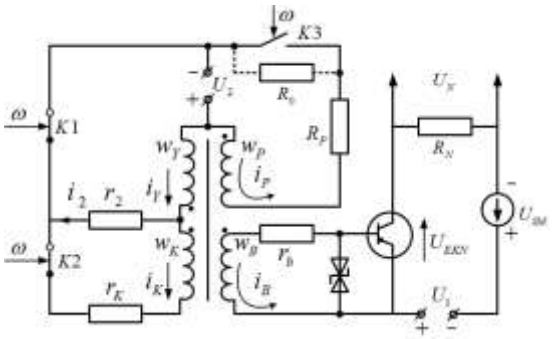

Figure 4. Magnetic transistor dividing device.

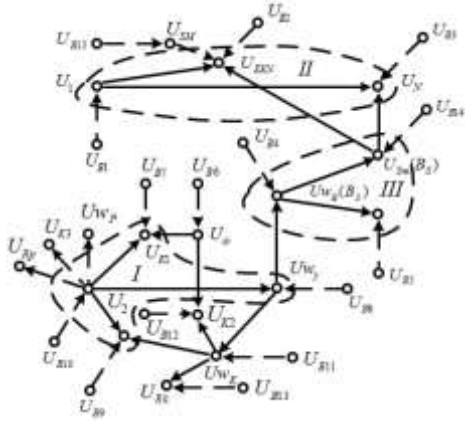

Figure 5: Causal graph of the MTDD.

From the CCGs we obtain the following system of MTDD error source sets, whose nature is described in [6]:

$$P_1 = \{U_{\text{wy}}, U_{\text{wb}}, U_{SM}, U_N\}; \quad (6)$$

$$P_2 = \{U_{k1}, U_{r2}, U_{\text{rb}}, U_{\text{EKN}}, U_{\text{wk}}, U_{k2}, U_{\text{Rk}}\}; \quad (7)$$

$$P_3 = \{U_1, U_2, U_\omega\}; \quad (8)$$

$$P_4 = \{U_{B1}, U_{B2},..., U_{B14}\} \quad (9)$$

As it follows from the set of P_1 (6) sources of errors, there are much less informative nodes in the direct information transmission path in the MTDD and this is due to the fact that the information transmission from the input node U_2 occurs in the control half-period of the basic amplifier, and the working half-period serves to return the cores to the initial position, thus the working half-period of the cores is not involved in the direct information transmission (Fig. 4).

Consider the accuracy characteristics of the MTDD associated with the route $U_2 U_{\text{wy}} U_{\text{wB}} U_{\text{SM}} U_N$ of the CGs. The top U_{K3} of the CGs represents the

voltage on the key K_3 of the MTDD (Fig. 4). The important parameter here is the reverse resistance of the transistor keys R_0. The final value of R_0 can cause a certain error in the output of this route. At the same time, new uninformative vertices of the graph appear, i.e. new sources of errors U_{R0}, U_{wp} and U_{Rp} (shown in Fig. 5 as dashed lines).

The expression for the core saturation angle θ_{Sp}, taking into account the inverse resistance R_0 of the K_3 switch, is determined by solving together the following system of (10):

$$\begin{aligned} i_2 w_y - i_K w_K - i_B w_B - i_P w_P &= Hl \\ U_2 &= -w_P s\omega \frac{dB}{d\tau} + i_P\left(R_P + R_0\right) \end{aligned} \tag{10}$$

With this system in mind:

$$i_P = \frac{U_2 + w_P s\omega \dfrac{dB}{d\tau}}{R_P + R_0}; \tag{11}$$

$$i_2 = \frac{Hl + i_K w_K + i_B w_B + i_P w_P}{w_y} \tag{12}$$

Substituting in (1.12) the expression for the currents and (1.11) from system (1.10) we obtain

$$U_2\left[1+\frac{r_2}{R_k}-\frac{r_2 w_k}{R_k w_y}-\frac{r_2 w_p}{(R_P+R_0)w_y}\right]=\frac{dB}{d\tau}w_y S\omega\left[1+\frac{r_2}{R_k}-\frac{r_2 w_k}{R_k w_y}+\frac{r_2 w_p^2}{(R_P+R_0)w_y^2}\right] \tag{13}$$

Let's introduce the notation:

$$\xi = 1 + \frac{r_2}{R_K} - \frac{w_K r_2}{w_y R_K}.$$

From (13) we then obtain the following expression for the saturation angle of a ferromagnetic core:

$$\theta_{Sp} = \frac{\pi U_S'\left[\xi + \dfrac{r_2 w_p^2}{(R_0 + R_P)w_y^2}\right]}{U_2\left[\xi - \dfrac{r_2 w_p}{(R_P + R_0)w_y}\right]}, \tag{14}$$

where $U_2 \geq U_S'$; U_S'- core saturation voltage;

Define the error caused by the non-ideality of transistor switch K_3 as $\delta_{\theta K3} = \theta_{Sp} - \theta_S$.

Decomposing the expression for θ_{Sp} and limiting it to the second term, we obtain:

$$\delta_{\theta K3} = \frac{\pi U_S}{U_2}\left[\frac{r_2 w_p}{\xi w_P (R_P + R_0)} + \frac{\dfrac{r_2 w_p^2}{(R_P + R_0)w_y^2}}{\xi - \dfrac{r_2 w_p}{(R_P + R_0)w_y}}\right]. \tag{15}$$

Given the error caused by the first route, for the average value of the load voltage of a two-half-period MTDD, we have

$$U_{Naver} = \frac{(\theta_S + \delta_{\theta K3})}{\pi}U_1 - \frac{(\theta_S + \delta_{\theta K3})}{\pi}\varphi_T\left|\ln\frac{\alpha_1}{1+\dfrac{I_{KN}}{(1+\beta)I_{б1}}}\right| + U_{Bf} \tag{16}$$

From where, the total absolute error of the MTDD is equal to:

$$\delta_{\Sigma Д} = \frac{U_S'}{U_2}\left[\left(\frac{1}{\xi K_0} + \frac{\dfrac{w_p}{w_y K_0}}{\xi - \dfrac{1}{K_0}}\right)U_1 - \varphi_T\left|\ln\frac{\alpha_1}{1+\dfrac{I_{KN}}{(1+\beta)I_{B1}}}\right|\right) - \varphi_T\left|\ln\frac{\alpha_1}{1+\dfrac{I_{KN}}{(1+\beta)I_{B1}}}\right|\Bigg] + U_{Bf} \tag{17}$$

where $K_0 = \dfrac{w_Y (R_0 + R_P)}{r_2 w_P}$.

Taking the following design values and parameters (Fig. 4) [12]:

$f = 50$ [Hz]; $U_{\text{Sm}} = 0.3$ [V]; $H_S = 10$ [A/m]; $I_{KN} \approx \dfrac{U_1}{R_N}$; $U_{1\max} = U_{2\max} = [10]$ V, $w_y = 150$ [W]; $w_p = 600$ [Wt]; $S = 25$ [mm²]; $R_p = 200$[Om]; $R_k = [176.5$ Om]; $R_N = [200$ Om]; $R_0 = 10^6$ [Om]; $r_2 = 100$ [Om]; $r_b = 30$ [Om] and not taking into account the high-order components of $\delta_{\Sigma Д}$, we obtain

$$\delta_{\Sigma_Д} = \frac{0.9}{U_2}\left(13.24\cdot 10^{-4}U_1 - 0.025\left|\ln\frac{0.95}{1+0.02U_1}\right|\right) \tag{18}$$

The error reduced to the full scale of the divider is equal:

$$\delta_{\Sigma_Д}\% = \frac{0.9}{U_2}\left(13.24\cdot 10^{-4}U_1 - 0.025\left|\ln\frac{0.95}{1+0.02U_1}\right|\right)\% \tag{19}$$

It can be seen from the calculated (Fig. 6) $\delta_{\Sigma Д}\% = F(U_1, U_2)$ [5], [9] MTDD relationship the highest error value in the dividing area corresponds to point A ($U_{1\max}, U_{2\max}$), and the sign of the error $\delta_{\Sigma Д}\%$ can change in the dividing area (ABCD[1]).

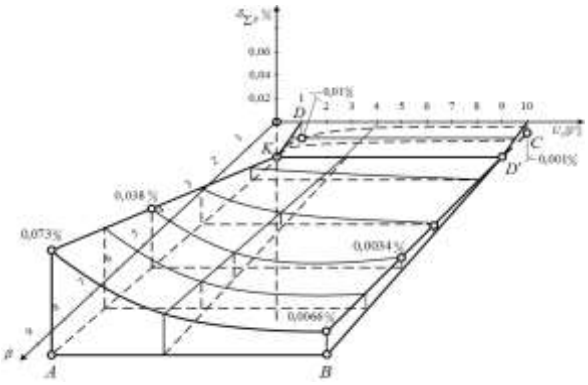

Figure 6: Calculated dependence of the total error on the input RC voltages.

The greater the ratio w_p/w_y, the greater the effect of reverse resistance R_0 of switch K_3. Decreasing this ratio, associated with increasing the number of turns w_y significantly reduces the multiplicity of change over the input U_2. We find such a value of input quantity U_1 (divisible), at which the total error $\delta_{\Sigma Д}\% \approx 0$ over the whole range of divisor change U_2. This value can be found from the condition: $13.24 \cdot 10^{-4} U_1 - 0.025 \left|\ln \frac{0.95}{1+0.02U_1}\right|$. From where $U_1 \approx 1.6$ V, at which the errors of the two divider CGs routes are mutually compensated. As U_2 increases, the total error decreases, and according to the law of inverse proportionality, $U_1 = \text{const}$. The total systematic error $\delta_{\Sigma Д}$ caused by non-ideality of U_{EKN} and U_{K3} vertices is a complex function that depends both on the many parameters of the magnetic part and on the parameters of the MTDD transistor keys, as well as on the parameters of the input and reference vertices of the CGs - U_1, U_2 and U_ω. Therefore, the total systematic error of the MTDU can be reduced by changing the following parameters:

- reducing the number of winding turns w_P, which reduces the effect of R_0 on the accuracy of the MTDD;
- reducing U_S by adjusting the parameters ω, S, B_S and w_y according to the design constraints.
- at higher reference oscillator frequencies, the influence of the $U_{\delta f}$ component, the total error, must also be taken into account.

During experimental research, the uncertainty of the MTDD did not exceed 0.2%. This error includes methodological and measurement errors, which are unavoidable in MTDD studies.

4 CONCLUSIONS

Based on the conducted research, the following main results and conclusions were obtained:

1) A methodology has been proposed for investigating the accuracy characteristics of devices, particularly FCs, using their CGs, which allowed us to systematise and classify the sources of error from a theoretical-multiple point of view.
2) It is established the position that the errors of devices in the "generalized top" of their CGs are subject to the basic laws of electric circuits, i.e. Kirchhoff's laws. This position makes it possible to develop a methodology for analysing the accuracy, parametric reliability and stability of both individual sections of an electrical circuit and devices as a whole.
3) The established provision on the errors of electrical circuits makes it possible to create a test system structure for analyzing accuracy, parametric reliability and stability, both of individual sections of circuits and devices as a whole.
4) The structural diagram of automatic error correction and accuracy testing based on CGs with the introduction of correction by individual vertexes of CGs devices makes it possible to develop new FCs with improved accuracy.

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