Low-Power Redundant-Transition-Free TSPC Dual-Edge-Triggered Flip-Flop with Single-Transistor Clocked Buffer

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Keywords: Dynamic Power, Dual-Edge Triggering, Flip-Flop.

Abstract: Designing low-power flip-flops with better reliability becomes crucial as the need for energy-efficient and high-performance integrated circuits continues to climb. A Low Power Redundant-Transition-Free True Single-Phase Clock (TSPC) Dual-Edge-Triggering Flip-Flop (DETFF) leveraging a Single-Transistor-Clocked Buffer (STCB) is developed and presented in this work as a new way to deal with these problems. With the goal of improving performance and reducing Low power consumption, the proposed design integrates the TSPC & DETFF optimums. architectures by reducing the number of redundant transitions during clocking and guaranteeing strong dual-edge triggering. An unique Single-Transistor-Clocked Buffer is also used to optimize the clock distribution network, which further contributes to power efficiency. Power consumption, speed, and dependability are some of the performance indicators measured by the flip-flop. These are assessed by comprehensive simulations conducted using technologies usually used in the industry. Testing the suggested architecture against current flip-flop designs shows that it is more efficient and reliable. Not to mention completely changing the game when it comes to low-power digital circuits design, the proposed Low Power Redundant-Transition-Free TSPC DETFF with Single-Transistor-Clocked Buffer has also made a substantial impact as an exciting new direction for future integrated circuits, which will require increased reliability and energy efficiency. Among the most potent building elements of processing in the GPU/AI era is the flip-flop (FF). An STC-based, dual-edge-triggered (DET) FF based on buffers is introduced to solve this problem. In the realm of data testing, STC support is great because it only needs one timed semiconductor and gets rid of all the internal and clock excess changes that other DET methods have. Approval for 22nm FD-SOI CMOS post-format recreations at 10% swapping movement.

1 INTRODUCTION

Power consumption is a major concern for CMOS advanced architecture, especially with GPU/AI brain network processor strain. calculate handling power used to make man-made intelligence copies 3.4 months from now [1]. Modern processor timing systems can account for up to 50% of the power consumption [2]. Streamlining power usage is a crucial aspect of addressing the previously mentioned power dispersion issue.

Clock distribution networks and flip-flops make up a processor's timing structure. A clock with only one stage FFs need more power to handle specific information since they process one clock edge at a time while addressing approaching information. Data is processed on both clock edges using dual-edge-triggering (DET) flip-flops. This allows them to continue operating at throughput even in the event of split clock recurrence.

Flip-flop is essential to modern devices and PC design. Parallel data storage and sequential rationale

circuit. Registers, counters, and memory components consistently use goes back and forth.

In the dynamic field of integrated circuit design, finding solutions that save energy is essential for keeping up with the demands of current electronic systems. With the trend towards increasingly integrated systems and lower process nodes, Power consumption is undoubtedly a significant problem. Since they are essential parts of digital circuits, flip-flops are crucial in deciding how well and how efficiently these systems work as a whole:

- The clock and internal redundant switching are omitted entirely from the proposed first DET FF.
- Our FF design recommends using STC buffers with no duplicate transitions. T.

This research introduces a novel design approach that addresses the dual challenges of low power consumption and reliability in flip-flop systems. We propose introducing a novel Low-Power Redundant-Transition-Free TSPC DETFF that combines the advantages of True Single-Phase Clock (TSPC) and Dual-Edge-Triggering Flip-Flop (DETFF) techniques. This design not only seeks to minimize unnecessary transitions during clocking but also leverages dual-edge triggering to significantly enhance speed and efficiency.

A Single-Transistor-Clocked Buffer (STCB) is introduced as a key element of the proposed design. Reducing power consumption even further without sacrificing the robustness needed for dependable circuit functioning, this feature optimizes the clock distribution network. Together, TSPC, DETFF, and STCB form a novel and all-encompassing strategy for designing high-performance flip-flops with minimal power consumption.

The importance of efficient and dependable flip-flops is growing as the semiconductor industry keeps moving the needle on miniaturization and integration. Discover a new development in this field as this research delves into the proposed Low Power Redundant-Transition-Free TSPC DETFF with Single-Transistor-Clocked Buffer and how it could shape the future of digital circuits that are energy efficient. Complete simulations and comparison studies prove this design's effectiveness, opening the door to improvements in low-power, high-performance integrated circuit designs.

Standard signals that synchronise activity on computer circuits and on flip-flops are abided by by clock beats. In response to a clock signal, a flip-flop can store or transfer data. The SR (Set-Reset) and D (Data) flip-flops are the two most prevalent types.

1.1 Sr Flip-Flop

Two sources of information and outcomes regarding.The SR flip-flop includes inputs for Set (S) and Reset (R), as well as outputs for Q and its complement (Q).It is possible to reset Q yield to 0 by activating the R input and to 1 by activating the S input. In contrast, Q∨ yield is used to address Q yield. It is probable that an SR flip-flop will experience a "race condition". When two data sources are active simultaneously, it results in an undefined state.

1.2 D Flip-Flop

The D flip-flop produces two signals, Q and $\overline{Q}$.which are complementary to each other. D (data) input is its only input. D input determines the state of Q output. When the clock signal is engaged, the D input is changed to the Q output. In response to a high (1) or low (0) D input, Q's output shifts from high to low. The inverse of Q output is $\overline{Q}$ output.

Frequently utilized for control, synchronization, and data storage, flip-flops are integral to digital systems. Connecting multiple flip-flops enables the construction of complex sequential circuits, such as registers and counters. These circuits form the foundation of digital systems and devices like computers, calculators, and communication devices. How sequential logic circuits like flip-flops react to clock signals is the subject of ideas like dual-edge and single-edge triggering.

1.2.1 Single-Edge Triggering

To maintain single-edge triggering, a flip-flop must permit changes to its state only on Often called rising-edge triggering, positive-edge triggering occurs at one edge of the clock signal. In positive-edge triggering, the flip-flop can't change its state until the clock signal crosses the rising edge, which is a low-to-high transition. While going from low to high, the flip-flop stays in the same state it was in before the rising edge. To activate their operations, 90% of digital systems rely on the previously indicated trigger.

1.2.2 Dual-Edge Triggering

While flip-flops can only change their state on one of the clock signal edges, dual-edge triggering allows them to do it on both. Everything that has been said so far proves that the flip-flop is capable of sampling input and updating its state anytime there is a change in the clock signal, be it a rising or falling edge. If designers are working on sequential logic circuits, the aforementioned choice gives them more leeway (Fig. 1).

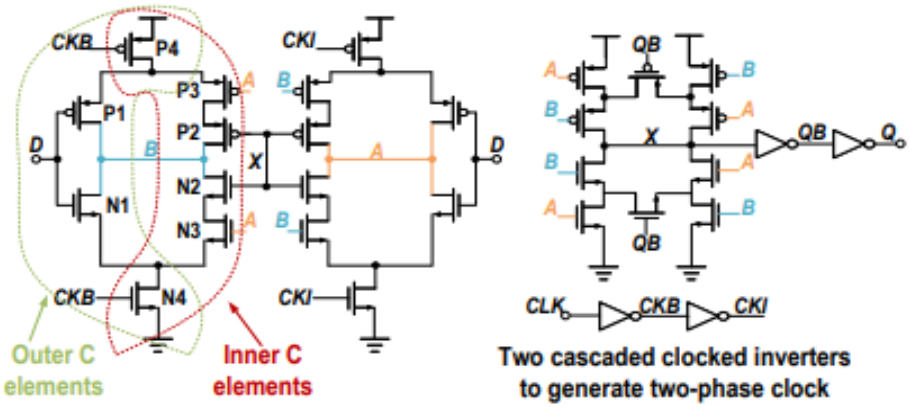

Figure 1: Element DET, floating node C, and FN C-DET.

Although dual-edge triggering isn't as common as single-edge triggering, it's still the go-to method for niche uses that demand pinpoint synchronization or timing.

The decision between single-edge and dual-edge triggering is determined by the specific application and design requirements. For most digital systems, single-edge triggering is effective and easy to implement. However, dual-edge triggering has its applications, among other things, designing fast circuits, implementing protocols, and controlling timing precisely.

1.2.3 Single Transistor Clocked Buffer

A basic digital circuit that is employed to amplify and transmit binary signals that are synchronized with a clock signal is a clocked buffer with a single transistor, sometimes called a single-stage clocked buffer or a latch with a single transistor. For driving and isolating signals across various circuit components, it finds extensive application in digital systems.Just one transistor Along with a clock signal, the single-transistor clocked buffer incorporates a metal-oxide-semiconductor field-effect transistor or complementary metal-oxide-semiconductor.

A periodic square wave, referred to as a clock signal, governs the buffer. The design specifies that the transistor will conduct and allow the input signal to flow towards the output whenever the clock signal is active, whether it's high or low. Transistor goes off, essentially separating, when clock signal is not active. An uncomplicated digital device capable of amplifying and distributing clock-synchronized binary signals is a clocked buffer that uses only one transistor, sometimes called a single-stage clocked buffer or a latch that uses only one transistor, commonly referred to as a single-transistor clocked buffer. Its primary function in digital systems is to drive and separate signals among various circuit components. In a single-transistor clocked buffer, The only components are the rhythmic signal and a solitary transistor, usually a field-effect transistor (FET) or a complementary metal-oxide-semiconductor (CMOS). It is the timer signal that controls the buffer's functioning and is characterised by a recurring square wave. The transistor conducts while the clock signal is active (either high or low, depending on the design), and permits the input signal to go through to the output. The transistor turns off and is practically disconnected from the circuit when the clock signal is not active.

2 LITERATURE SURVEY

The desire for energy-efficient integrated circuits has encouraged low-power flip-flop design developments. Numerous methods and architectures have been developed to reduce power usage and preserve reliability. We review the literature that supports the proposed "Low Power Redundant-Transition-Free TSPC Dual-Edge-Triggering Flip-Flop using Single-Transistor-Clocked Buffer" and contextualize its contributions.

2.1 Traditional Flip-Flop Architectures

Key digital circuit components include master-slave and D-type flip-flops. These frequently used designs are power inefficient, especially with redundant transitions and static power waste during idle states.

2.2 The True Single-Phase Clock (TSPC)

The flip-flop architecture addresses power limitations in previous systems. TSPC saves power and runs faster. Minimising unnecessary transitions and boosting reliability remain difficulties.

2.3 Dual-Edge-Triggered Flip-Flops (DETFF)

These architectures are renowned for their ability to operate on both rising and falling clock edges, resulting in a threefold increase in data transfer rates. This trait improves speed and performance, but power consumption and dependability must be balanced.

2.4 Clock Distribution Networks

Digital circuits rely on clock distribution networks, which impact power consumption and signal integrity. Single-Transistor-Clocked Buffers (STCB) have been studied to optimise clock distribution and reduce power overhead.

2.5 Low-Power Redundant-Transition-Free Flip-Flops

Many recent flip-flop designs aim to reduce redundant transitions during clocking occurrences. These designs aim to reduce dynamic power consumption and boost efficiency, paving the way for more complete flip-flop systems.

We identify gaps and obstacles that our suggested "Low Power Redundant-Transition-Free TSPC DETFF using Single-Transistor-Clocked Buffer" addresses by reviewing the research in three important areas. We situate our work within the context of improving low-power, high-performance flip-flop topologies for next-generation integrated circuits by comprehending the state-of-the-art.

3 METHODOLOGY

In terms of intensity and concession, snares and flip-flops are the most important components of an arrangement. They classify different kinds of definite and express heartbeat ages, alongside static and semi-dynamic returns with a single edge set off. We provide an ip-DCO, an implicit pulse, semi-dynamic flip-flop, which incorporates the quickest delay of each flip-flop plus a large amount of non-positive setup time information. On the other hand, for the majority of mission-critical pathways in an organization, an explicit-pulsed static flip-flop (ep-SFF) is the smartest energy-saving option [3].

Two edge-set off back-sells are being considered for potential power use. Certain conventional two-edge-set off layouts are found to be unfit for basic uses due to their dull appearance and excessive district discipline. One additional express beat double-edge-set off flip-flop Introduces a comparable value to a single-edge-triggered structure with much reduced power consumption in the networks that control flip-flops and clock movements [4].

Specifically, New Dual-Edge-Triggered (DET) flip-flops that are long-lasting and use less power are proposed in this study. By taking input data at both clock edges, DET-FFs can dramatically improve energy efficiency using the traditional Single-Edge-Triggered (SET) method. Dynamic voltage scaling, when used in tandem, should significantly improve efficiency. Previous DET-FF plans were limited to low voltage frameworks due to their inherent insensitivity to PVT (Process, Voltage, and Temperature) variations. For reliable performance at voltages as low as those in a neighboring edge framework, it is recommended to use a fully static certified single-stage coordinated DET-FF [5]-[7].

To address clock skew concerns and enable low-power operation, we employ a True-Single-Phase-Clocking (TSPC) architecture instead of the standard two-stage clocking strategy used in common DET-FFs. In addition, the low-voltage framework is guaranteed to operate reliably by the totally static implementation. This DET-FF is designed to work with 28nm CMOS technology. on the path to additional improvements in support arrangements, an intensified evaluation is planned that incorporates post-plan Monte Carlo simulation is employed to cover extensive Process, Voltage, and Temperature (PVT) ranges. Based on thorough testing and evaluation in comparison to previous DET-FFs, The proposed DET-FF demonstrates functionality at an impressively low voltage of approximately 0.28 V across a temperature range spanning from -40 °C to 120 °C. This is achieved while maintaining nearly optimal energy efficiency and power-delay product [8]-[12].

The utilization of dual-edge-triggered (DET) assisted operation presents an intriguing option for low-power, standard execution strategies. At the clock repeat stage, DET action can produce throughput comparable to that of conventional single-edge synchronous systems. In the workplace, an organization's regular contributions to overall power

usage can result in significant savings. Registers with specific model data on both clock edges should remain consistent and perform dual-edge-triggered (DET) operations reliably.

These registers are more disorganised and frequently encounter clock cross-talk between the internal revised clock and the primary clock, in contrast to their single-edge counterparts. The aforementioned crossing. Especially when operating with scaled power supplies and under process variations commonly observed in nanoscale advancements, might cause disagreements among cells and problems with reasoning. The unique static DET flip-flop (DET-FF) presented in the aforementioned paper completely avoids clock skew issues with a real single-stage clock because it doesn't require a changed clock edge for value. Although conventional DET-FFs fail miserably at low-voltage working locations, the suggested DET FF performed admirably when implemented in a conventional 40nm CMOS development. At a close edge supply voltage of about 500 mV, the proposed cell gives the smallest power-delay-thing and a 35% reduction in CK-to-Q latency, all while ignoring any remaining DET-FF executions [13].

Our investigation into possible power savings entail transitioning from conventional single-edge-triggered (SET) flip-flops to dual-edge-triggered (DET) flip-flops, as discussed in the aforementioned work. In the aforementioned study, we introduce a new family of D-type double-edge set-off algorithms that, unlike previous plans, use significantly fewer semiconductors in their execution. The process of power dissipation in these flip-flops and single-edge-triggered flip-flops is investigated through building-level tests, logical reflections, and simulations. The effect of data successions on energy distribution regarding single and double edge set off back-pedals is remembered for investigation in an autonomous execution focus. We next look at the possibility of achieving framework-level energy reserve funds by switching from registers built about single-edge set off back-peddles to registers produced about two-edge set off back-peddles.

The results remain highly promising, illustrating that specific dual-edge-triggered flip-flops can achieve significant energy savings with minimal complexity. Low-energy dual-edge-triggered flip-flops are presented in the aforementioned paper [15] using a creative execution method. The new approach employs a clock branch-sharing plan in an effort to reduce the number of timed semiconductors in the design. There are two other approaches that have recently been suggested for use in limiting hinder and exchanging actions: part way and contingent release. The latest CBS IP configuration outperforms other state-of-the-art dual-edge-triggered flip-flop designs in terms of power consumption (up to 20%) and power degradation probability (up to 12.4%) [16].

One significant drawback of integrating D-type dual-edge-triggered flip-flops (DET-FFs) into VLSI framework design is the need for a substantial quantity of semiconductors. Two new DET-FF circuits, one static and one dynamic, reduce the semiconductor count to a level comparable to that of specific conventional single-edge-triggered flip-flops (SET-FFs).In addition to functioning well at high frequencies, these novel circuits are easy to use, have a transparent architecture, and are very resistant to race and metastability problems (static and dynamic). The use of DET-FFs in the configuration of VLSI frameworks is more widespread, promising, and applicable due to these reasons [17].

According to the 2008 Global Innovation Guide for Semiconductors, power consumption is one of the three primary issues and a major cause of performance bottlenecks in systems. A significant amount of on-chip power is consumed by the clock framework in real-world use. This framework consists of failure flops and the clock circulation organisation. the aforementioned article discusses several near-term configuration draws for low-power timing frameworks. Using fewer timed semiconductors is one of the most effective strategies to To alleviate the clock load limit, we introduce a timed pair—an innovative flip-flop design that decreases the number of surrounding timed semiconductors by approximately 40%. This approach enables a 24% reduction in the power needed to drive the clock. Furthermore, through the integration of low swing and double-edge timing, these novel flip-flops can be seamlessly incorporated into timing frameworks [11]-[14].

The static dual-edge-triggered (DET) flip-flop designs described in the previous study exhibit remarkable circuit behavior since C-components are consistently used in them. Two better execution strategies improve the standard Hook MUX DET flip-flops, making them immune to signal intensity fluctuations at any point in their internal circuits. These enhancements help bring five first-rate DET flip-flops to market. The low-energy propagation that comes with flip-flops is a typical result of input errors. A comparison is made between new dual-edge-triggered (DET) flip-flops and existing DET flip-flops using replication in a high-performance 28 nm CMOS technology. The new flip-flops demonstrate better features, such as an indeterminate

power-delay product (PDP), across several exchange-related jobs. Through rigorous voltage scaling and Monte Carlo simulations, we confirm that the proposed designs are resilient against Process, Voltage, and Temperature (PVT) fluctuations [18].

The Advanced High-performance Bus, a high-performance member of the AMBA bus family, which stands for Advanced Microcontroller Bus Architecture. The components that make up a framework should be able to communicate with one another. ARM defines AHB standards, which provide communication between on-chip processors and external memory interfaces located off-chip. An AHB framework that can support four slaves and one expert is detailed in the aforementioned study, along with its design and implementation. the aforementioned work is the basis for the AHB Convention's building blocks, which include multiplexers, slaves, decoders, and bosses. The aforementioned AMBA-AHB convention can be used into any application so long as the strategy aligns with AHB principles. The following architectural components are commonly seen in Verilog systems: nurture experts, slaves, decoders, and multiplexers. To promote an environment conducive to confirmation, System Verilog (SV) is employed. Using Coach Designs' High Level Confirmation Apparatus, QuestaSim, the plan is duplicated, checked, and code and valuable inclusions are registered the third.

4 EXISTING STATE OF THE RESEARCH ENDEAVORS

Documentation of Just One Change Double-Edge-Triggered flip-flop is abbreviated as STCDET. Several benefits are offered by the aforementioned style of flip-flop design in comparison to more conventional designs.

Higher data transfer rates are still within reach when using STCDET flip-flops instead of single-edge-triggered ones. By collecting data on the rising and falling edges of the clock in a single clock cycle, STCDET flip-flops allow for quicker and more efficient data processing, virtually doubling the data transfer rate.

Variations in the timing of clock signals, or clock skew, can affect the reliability and performance of flip-flops. With two clock edges used to capture data, STCDET flip-flops are less susceptible to clock skew. aforementioned mitigates the effect of clock skew on flip-flop timing needs. Improved Resistance to Noise: STCDET flip-flops exhibit enhanced resistance to noise.in opposition to flip-flops that just have one edge trigger. Their resistance to clock signal noise and hiccups is due to the fact that they capture data on both clock edges. the aforementioned noise immunity helps keep data intact and decreases the chance of incorrect data collecting.

In comparison to other flip-flop designs, STCDET flip-flops are able to achieve lower power consumption. It is still possible to get greater data transfer rates with STCDET flip-flops as opposed to single-edge-triggered flip-flops. Because STCDET flip-flops can capture data on both the rising and falling edges of the clock within a single clock cycle, they virtually double the data transmission rate, allowing faster and more efficient data processing. This achievement can be further enhanced with power optimization techniques like clock gating, made possible by a decreased vulnerability to clock skew.
It is possible to do simpler timing analyses for STCDET flip-flops than for flip-flops with more intricate designs. Meeting time constraints is feasible because data is captured on both the positive and negative edges of the clock in a single clock cycle. The design process is streamlined and made easier. aforementioned may result in versions of the design that are both faster and more efficient.

One approach to making them backward compatible with STCDET flip-flops (Fig. 2) [19], is to implement single-edge-triggered flip-flops. All of the above makes it possible to incorporate them into preexisting digital systems without disrupting the system's overall architecture or necessitating huge changes.

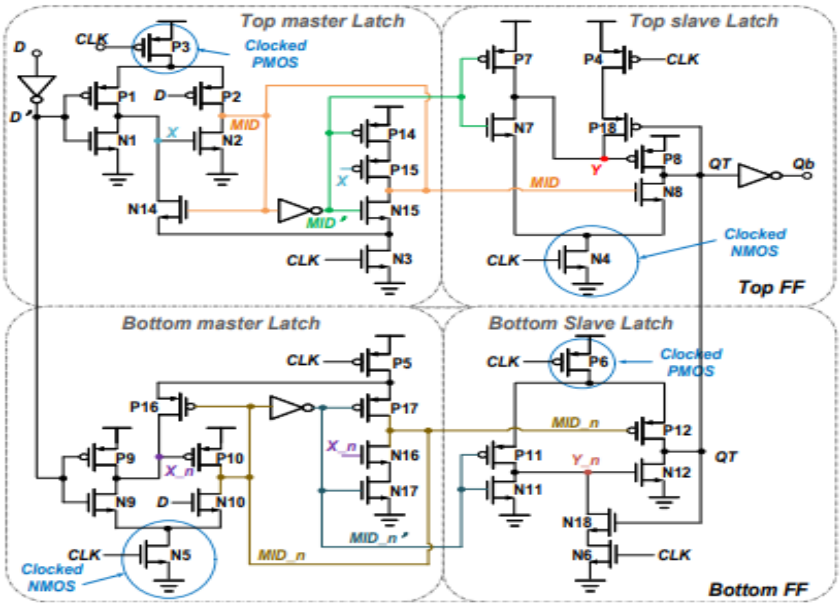

Figure 2: Schematic of the proposed TSPC-DET flip-flop.

4.1 Proposed

A decrease in the edge voltage of CMOS circuits brought on by voltage scaling increases the subthreshold leakage current and, eventually, static power scattering. We provide LECTOR, a short-circuite method for fabricating CMOS doors, which significantly reduces leakage current while increasing unique power dispersion. One method that has been suggested is to place two semiconductors for controlling leakage – a p-type and an n-type transistor are placed within a logical gate, with one set of terminals for each type being connected to the other's source. In the mentioned architecture, one of the LCTs is consistently "close to its end voltage" irrespective of the mix of data sources. This reduces leakage currents by reducing the path's resistance from V/sub dd/ to ground, as indicated before. A static CMOS complex door execution is the initial step in creating a spillage controlled circuit from an entry-level netlist regarding the given circuit. Once added, LCTs remain. LECTOR's primary value is in the fact that, in contrast to competing methods, it effectively reduces leakage regardless of whether the circuit is active or not (Fig. 3). In complementary metal-oxide-semiconductor (CMOS) circuits, voltage scaling reduces the edge voltage, which increases the subthreshold leakage current and the static power dissipation.

The LECTOR method, which we propose, provides a novel approach to reducing leakage current in CMOS doors while enhancing dynamic power scattering. Integrating a p-type and an n-type leakage control transistor (LCT) into a logical gate is a critical part of the previously described approach. The gate terminal of each LCT is controlled by the source of the corresponding semiconductor. Following the aforementioned approach, LCTs are typically "close to their end voltage" regardless of the data mix. This reduction in leakage currents is fundamental, the aforementioned increases blockage in the way from V/sub dd/to ground correspondingly.

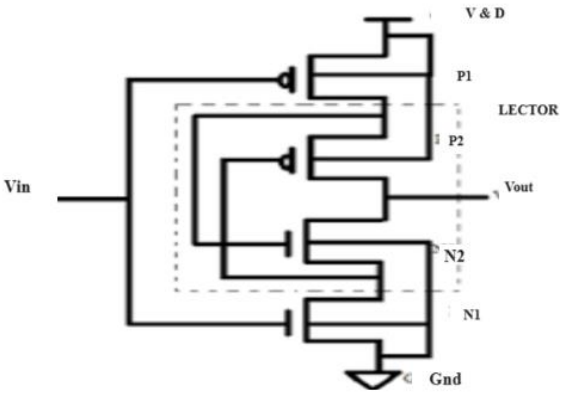

Figure 3: Schematic about LECTOR.

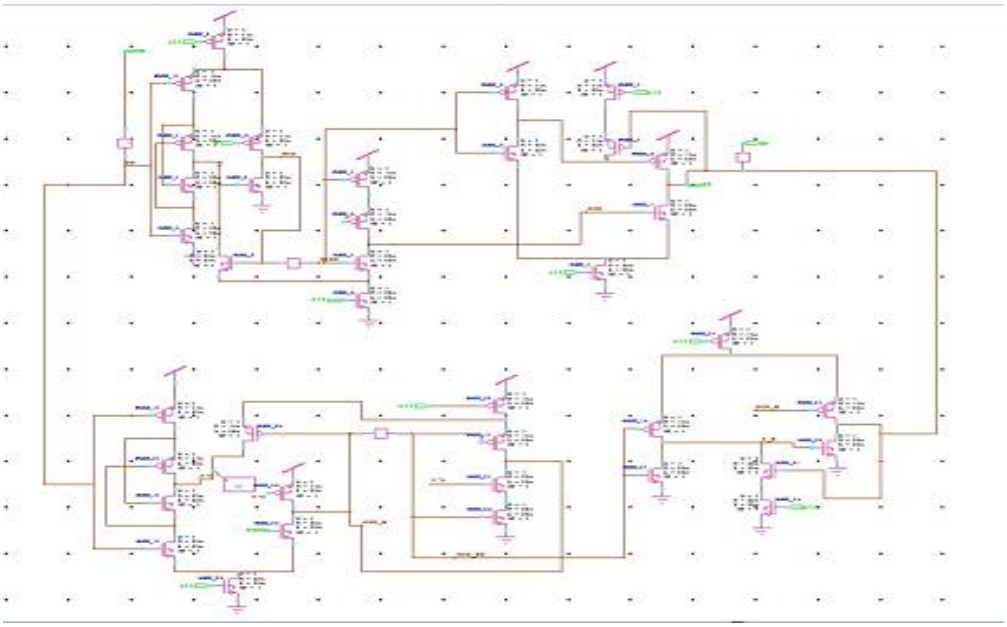

Figure 4: Schematic about TSPC STCDET using LECTOR.

4.2 Operation about Top FF in STC-DET

When C L K = 0, as shown in the worked-on reasoning diagram in Figure 5a, The transistors (P2, N2) effectively function as a virtual inverter. The upper master hook's timed PMOS P3 activates when CLK = 0, causing node X to transition to D'. Conversely, in the upper slave hook of Figure 4, the timed NMOS N4 remains off due to CLK = 0, indicating that node Y will not reach 0, and PMOS P8 is also off. Later on, data is sent to M I D via the top expert lock (bolt in the top left corner of the previous illustration). Due to the inability of VDD and QT to interface with either GND, the top FF's QT is drifting (refer to the upper left corner of Figure 5a).

Figure 4 depicts a negative-set off STCB comprising of semiconductors N1, N2, P1, P2, and P3. The sign testing channel is a single coordinated semiconductor, P3. Unlike STCDET, FN_C DET and FS-TSPC (Fig. 3) exhibit a resistance-temperature (RT) component between a timing PMOS and a timing NMOS. Similarly, there is no discrepancy. The upper master latch (located in the upper left of Fig. 4) features a clock-driven NMOS transistor (N3), although it's used for guarding rather than data analysis. Regarding semiconductor P3, its timing is similar to certain. A bolt is shown in Figure 4 to exhibit the definite abide timing of four semiconductors (P3, N4, N5, and P6) as they all abide on the same information testing method. Using semiconductors (N4, N7, N8, P7, P8), top FF develops an additional sure set off STCB.

At CLK=1, the timed PMOS P3 is off, hence the routes leading to P1 and N2 in Figure 4's upper master latch are also off. Attendant (N3, N15, P14, P15) maintains reasonable territory regarding M I D in the same manner as indicated earlier. The pull-down guardian (N14, N3) will maintain X in its current state while its rationality state is 0. However, Y becomes M I D″ when the anticipated NMOS, N4, activates in the top slave lock. Using semiconductors (N8, P8) as a virtual inverter, we can change the state from MID—the only possible state before the clock's rising edge—to QT. Therefore, the top flip-flop is activated at the positive edge of the clock.

4.3 Operation of Bottom FF in STC-DET

Base master latch triggers (bottom left in Figure 4 occur when CLK = 0 in the base flip-flop, clock NMOS, and N5. Consequently, the specific connections to N9 and P10 remain dormant, and the protector (N16, N17, P5, P17) maintains MID_n's pristine logical condition. When the attendant (P16, P5) is sure that X_n is 1, they will protect the rational territory surrounding it. However, at the top of the image, the planned PMOS P6 switches on at Here, in the base slave latch (bottom right in Fig. 4), CLK is set to 0. This transforms Y_n into MID_n', which is similar to MID_n but not quite. The subsequent

realization of the P12 and N12 virtual inverter functions causes the generation of the MID_n signal, which is the second MID_n and the leading edge of the clock as it approaches QT (see bolt in the left half of Figure 5b). That being the case, the base flip-flop is secured by the negative edge of the work.

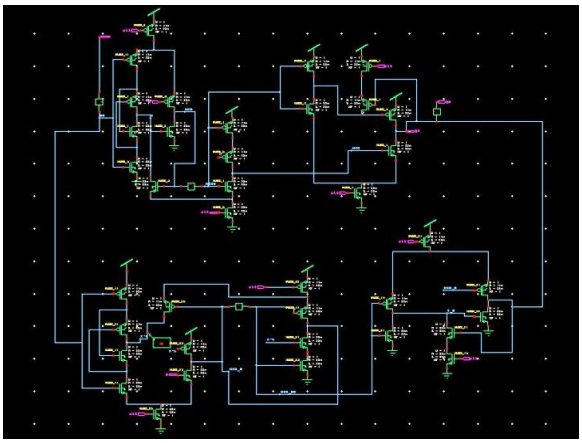

Figure 5: Schematic for STCDET using LECTOR.

5 RESULT AND ANALYSIS

Figures 5 and 6 present the outcomes of the Time-Shifted Pre-Charge (TSPC_DET) in the STCDET system using the novel LECTOR technique.

The diagram depicts an STCDET design utilizing the LECTOR approach, which reveals a notable reduction in power consumption.

The inner workings of an STCDET system that uses LECTOR technology, as explained in Figure 7, are shown below with corresponding simulation waveforms.

The following Figure 8 shows the spatial arrangement of the suggested circuit, referred to as Time-Shifted Pre-Charge (TSPC) in Self-Timed Content-Addressable Memory (STCDET).

The graphic depicts the project's power consumption metrics by offering a comprehensive overview of the power values associated with its execution, as shown in Figure 9.

We also provide a comparision table between proposed and extendsion (Table 1).

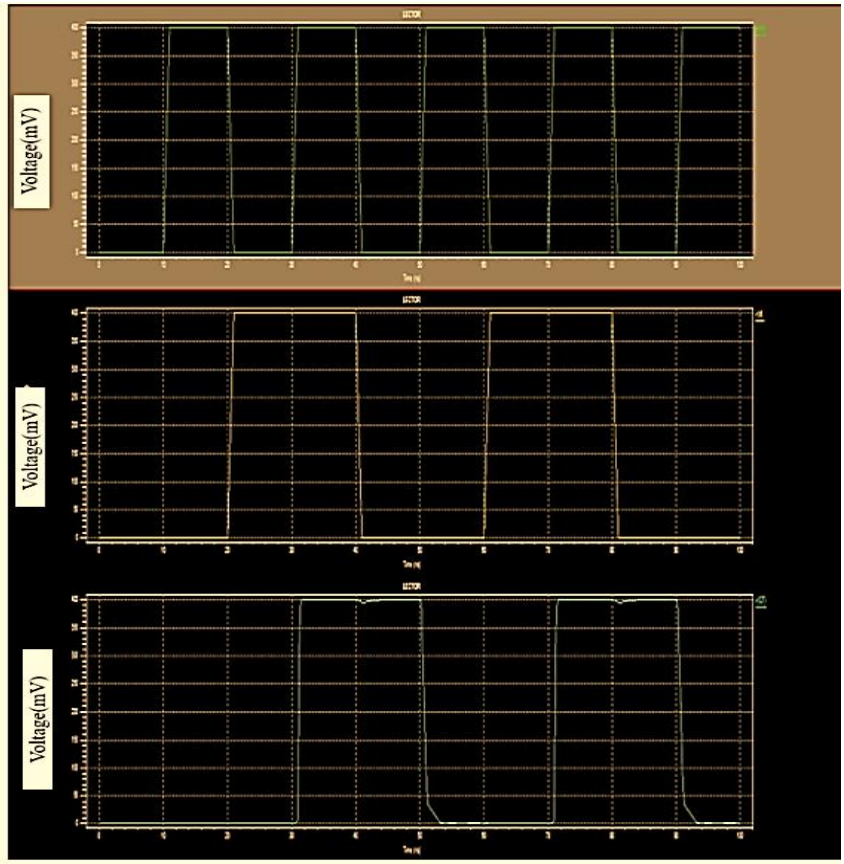

Figure 6: Waveform of STCDET circuit with LECTOR approach.

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* Device and node counts:
          MOSFETs - 54
          BJTs    - 0
          MESFETs - 0
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Figure 7: Area.

```
Power Results
vl from time 0 to 1e-007
Average power consumed -> 1.206081e-007 watts
Max power 1.861622e-006 at time 3.1223e-008
Min power 1.793915e-008 at time 4e-008
```

Figure 8: Power value.

```
delay = 2.0820e-008
    Trigger = 1.0250e-008
    Target  = 3.1070e-008
```

Figure 9: Delay value.

Table 1: Comparision table.

	AREA	POWER	DELAY
PROPOSED	42	1.886586e-007W	2.0205e-008
EXTENSION	54	1.206081e-007W	2.0820e-008

6 CONCLUSIONS

Built on the assurance that it entirely eliminates redundant transitions in double edge-triggered flip-flops using STC buffers, STC-DET is introduced as a new Low-power flip-flop that is triggered by both edges and does not undergo repeated transitions. Both positive-edge and negative-edge triggers are part of its environmental context. Different from earlier DET frameworks, STC eliminates all clock repeating sections, modifications, and internal surplus advances between two timed semiconductors. With everything else being equal, The information testing circuit for each positive-edge-triggered and negative-edge-triggered STC buffer has precisely one corresponding semiconductor. Additionally, the designed STC-DET is entirely transparent. To facilitate efficient data exchange among all DET designs, STC-DET minimizes power consumption throughout the board at different voltages for operation. The suggested STC-DET achieves the lowest power consumption in the normal switching activity range among all state-of-the-art DET flip-flops. However, applying the LECTOR method to STCDET can still further reduce power consumption.

REFERENCES

[1] S. Lapshev and S. M. R. Hasan, "New low glitch and low power DET flip-flops using multiple C-elements," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 63, no. 10, pp. 1673-1681, Oct. 2016.

[2] J. Tschanz, S. Narendra, Z. Chen, S. Borkar, M. Sachdev, and V. De, "Comparative delay and energy of single edge-triggered and dual edge-triggered pulsed flip-flops for high-performance microprocessors," in Proc. ISLPED, 2001, pp. 147-152.

[3] A. Karimi, A. Rezai, and M. M. Hajhashemkhani, "A novel design for ultra-low power pulse-triggered D-flip-flop with optimized leakage power," Integration, vol. 60, pp. 160-166, Jan. 2018.

[4] G. Lee, S. Shin, and Y. Lee, "A fully static true-single-phase-clocked dual-edge-triggered flip-flop for near-threshold voltage operation in IoT applications," IEEE Access, vol. 8, pp. 40232-40245, 2020.

[5] R. Hossain, L. D. Wronski, and A. Albicki, "Low power design using double edge triggered flip-flops," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 2, no. 2, pp. 261-265, Jun. 1994.

[6] H. You, J. Yuan, Z. Yu, and S. Qiao, "Low-power retentive true single-phase-clocked flip-flop with redundant-precharge-free operation," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 29, no. 5, pp. 1022-1032, May 2021.

[7] P. Zhao et al., "Low-power clocked-pseudo-NMOS flip-flop for level conversion in dual supply systems," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 17, no. 9, pp. 1196-1202, Sep. 2009.

[8] A. Bonetti, A. Teman, and A. Burg, "An overlap-contention free true-single-phase clock dual-edge-triggered flip-flop," in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), May 2015, pp. 1850-1853.

[9] M. W. Phyu, K. Fu, W. L. Goh, and K. S. Yeo, "Power-efficient explicit-pulsed dual-edge triggered sense-amplifier flip-flops," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 1, pp. 1-9, Jan. 2011.

[10] M. W. Phyu, K. Fu, W. L. Goh, and K. S. Yeo, "Ultra-low power pulse-triggered CNTFET-based flip-flop," IEEE Trans. Nanotechnol., vol. 18, pp. 756-761, 2019.

[11] P. Zhao et al., "Low-power clocked-pseudo-NMOS flip-flop for level conversion in dual supply systems," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 17, no. 9, pp. 1196-1202, 2009.

[12] H. M. Naser, O. A. Al-Ani, M. F. Mosleh, and F. Arith, "Umbrella-Shaped Wideband MIMO Wireless Communication Antenna," J. Telecommun., vol. 5, no. 4, pp. 46-53, Dec. 2023.

[13] A. Bonetti, A. Teman, and A. Burg, "An overlap-contention free true-single-phase clock dual-edge-triggered flip-flop," in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), 2015, pp. 1850-1853.

[14] I. H. Abed and S. Bahadori, "Using Density Criterion and Increasing Modularity to Detect Communities in Complex Networks," Int. J. Data Sci., vol. 2, no. 1, pp. 1-15, Jan. 2025.

[15] R. Hossain, L. Wronski, and A. Albicki, "Low power design using double edge triggered flip-flops," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 2, no. 2, pp. 261-265, 1994.

[16] P. Zhao et al., "Low-power clock branch sharing double-edge triggered flip-flop," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 15, no. 3, pp. 338-345, 2007.

[17] A. Gago, R. Escano, and J. Hidalgo, "Reduced implementation of D-type DET flip-flops," IEEE J. Solid-State Circuits, vol. 28, no. 3, pp. 400-402, 1993.

[18] S. V. Devarapalli, P. Zarkesh-Ha, and S. C. Suddarth, "A robust and low power dual data rate (DDR) flip-flop using C-elements," in Proc. Int. Symp. Qual. Electron. Design (ISQED), 2010, pp. 147-150.

[19] B. M. Krishna, J. Kalyani, Y. Venkatesh, V. Balaji, T. Umamaheswari, and Y. Srivalli, "An Efficient Low-Power Redundant-Transition-Free TSPC Dual-Edge-Triggering Flip-Flop Using Single-Transistor-Clocked Buffer," International Journal for Modern Trends in Science and Technology, vol. 10, pp. 369–376, 2024.